

# MOSTEK

## TOP OCTAVE FREQUENCY GENERATOR

### MK50240 / 1 / 2P / MK 50240 / 1 / 2N

June 1976

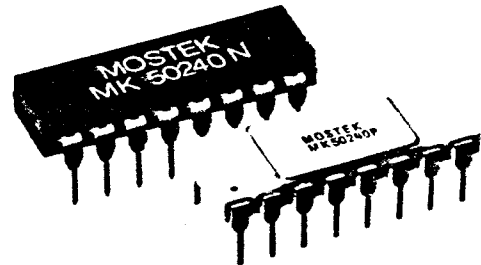
#### FEATURES

- Single Power Supply
- Broad Supply Voltage Operating Range
- Low Power Dissipation
- High Output Drive Capability

MK 50240 – 50% Output Duty Cycle

MK 50241 – 30% Output Duty Cycle

MK 50242 – 50% Output Duty Cycle



#### DESCRIPTION

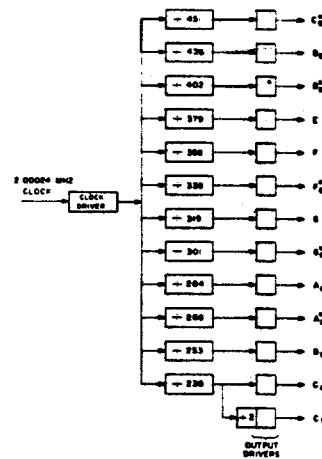
The MK 50240 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple  $12\sqrt{2}$  providing a full octave plus one note on the equal tempered scale.

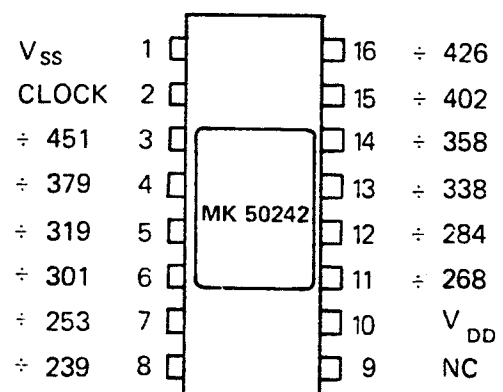
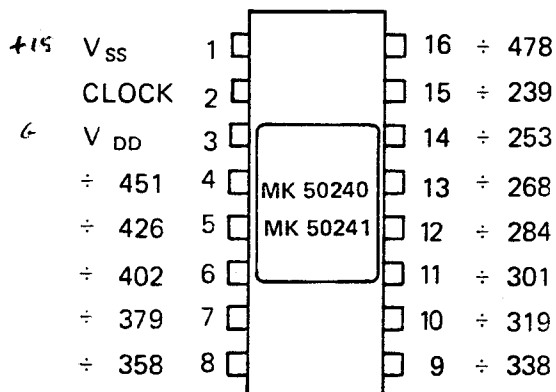
Low threshold voltage enhancement-mode, as well as depletion-mode devices, are fabricated on the same chip allowing the MK 50240 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600mW of power. The circuits are packaged in 16-pin dual in-line packages.

RFI emanation and feed-through is minimized by placing the input clock between the  $V_{DD}$  and  $V_{SS}$  pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the RF harmonic content of each output signal.

#### FUNCTIONAL DIAGRAM



#### PIN CONNECTIONS



## ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V <sub>SS</sub> .....	+0.3V to -20V
Operating Temperature (Ambient) .....	0°C to 50°C
Storage Temperature (Ambient) .....	-40°C to 100°C

## RECOMMENDED OPERATING CONDITIONS (0°C ≤ T<sub>A</sub> ≤ 50°C)

PARAMETER		MIN	TYP	MAX	UNITS	FIGURE
V <sub>SS</sub>	Supply Voltage	0		0	V	
V <sub>DD</sub>	Supply Voltage	-11.0	-15.0	-16.0	V	

## ELECTRICAL CHARACTERISTICS

(0°C ≤ T<sub>A</sub> ≤ 50°C; V<sub>SS</sub> = 0, V<sub>DD</sub> = -11 to -16V unless otherwise specified)

PARAMETER		MIN	TYP	MAX	UNITS	FIGURE
V <sub>IL</sub>	Input Clock, Low	0		-1.0	V	FIG. 1
V <sub>IH</sub>	Input Clock, High	V <sub>DD</sub> + 1.0		V <sub>DD</sub>	V	
f <sub>i</sub>	Input Clock Frequency	100	2000.240	2500	kHz	
t <sub>r</sub> , t <sub>f</sub>	Input Clock Rise & Fall Times 10% to 90% @ 2.5 MHz			30	nsec	FIG. 1
t <sub>on</sub> , t <sub>off</sub>	Input Clock On and Off Times @ 2.5 MHz		200		nsec	FIG. 1
C <sub>i</sub>	Input Capacitance		5	10	pF	
V <sub>OH</sub>	Output, High @ .70 mA	V <sub>DD</sub> + 1.5		V <sub>DD</sub>	V	FIG. 2
V <sub>OL</sub>	Output, Low @ .75 mA	V <sub>SS</sub> - 1.0		V <sub>SS</sub>	V	FIG. 2
t <sub>ro</sub> , t <sub>fo</sub>	Output Rise & Fall Times, 500 pF Load	250		2500	nsec	FIG. 3
t <sub>on</sub> , t <sub>off</sub>	Output Duty Cycle MK 50240P & MK 50242P MK 50241P (Pin 16 50%)		50 30		% %	
I <sub>DD</sub>	Supply Current		24	37	mA	outputs unloaded