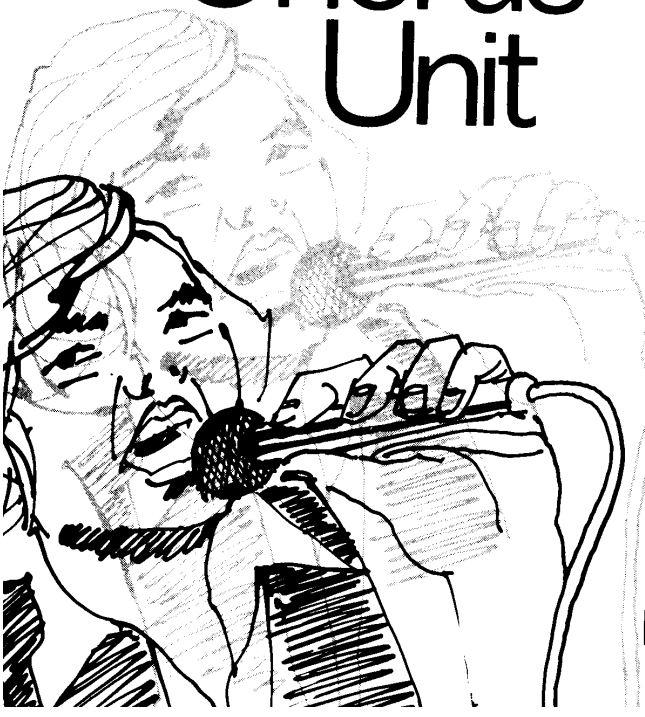
Mini Chorus Unit



THE mini chorus effect is one that receives a great deal of use these days, and it is probably used most by vocalists although it is also perfectly suitable for use with electronic instruments. The effect is basically very simple, and is produced by mixing a delayed signal with an undelayed signal, and the length of the delay is usually varied at a low frequency. Apart from varying the degree to which the two signals are out of synchronisation, this varying of the delay also gives a degree of vibrato to the delayed signal. The resultant audio output gives the impression that there are two instruments or vocalists singing or playing in unison, and this normally gives a much richer and more interesting sound. This effect should not be confused with the more complex chorus effect which uses more than one delay circuit and gives the impression of many vocalists or instruments using a single source.

BLOCK DIAGRAM

The block diagram Fig. 1 shows the various stages of which the Mini Chorus unit is comprised. The delay line is of the usual charge coupled (bucket brigade) type, and this provides a delay that is governed by the frequency of a two phase clock oscillator. A delay of 10ms or more is needed in order to give the desired double output effect, and in practice a delay which is varied from about 10ms to 20ms or so is perfectly satisfactory. A low frequency sweep oscillator is used to frequency modulate the clock oscillator and give the required variation in the delay time.

The delay required in this application can be obtained using a 512 stage delay line, but as the delay time is equal to the number of delaying stages divided by twice the clock frequency (in Hertz), this would give a clock frequency range of approximately 12 to 25kHz. This would give a rather restricted bandwidth since the maximum input frequency should be no more than half the clock frequency, and should preferably be no more than a third of the clock frequency. In order to obtain reasonable output quality this would give a maximum bandwidth of only about 4kHz. Filters are used at the input and output of the delay line to remove input signals at frequencies above the acceptable maximum input frequency, and to remove the clock signal (which effectively modulates the output signal) at the output. With a minimum clock frequency of about 12kHz both filters would need to have a very high level of performance in order to give satisfactory results.

It was therefore decided to use a 1024 stage delay line which is admittedly a little more expensive than a 512 stage type, but gives a more respectable bandwidth of about 8kHz, and with a clock frequency range of about 24 to 50kHz puts less stringent requirements on the input and output filters.

CIRCUIT

Fig. 2 shows the circuit diagram of the filter, delay line, and mixer stages of the unit.

The input filter is an active type which is based on TR1 and has a nominal roll-off rate of 12dB per octave and a cut-off frequency of approximately 9kHz. The output filter is essentially the same, but the emitter follower transistor is a *pnp* type instead of an *npn* device, and it is biased from the output of the delay line rather than from a potential divider.

The delay line integrated circuit is an SAD1024A which actually contains two 512 stage delay lines which are independent apart from common supply pins. R8 and R9 are used to bias the input of the first section of IC1 and C4 couples the output from TR1 to the input of this section. One output of the first delay line section (pin 11) is connected to the positive supply rail in accordance with the i.c. manufacturers' recommendations, and the other output (pin 12) is coupled to the input of the second section of IC1 by R10 and C5. C5 is needed as there is a small but significant d.c. shift through each delay line, and the second section of IC1 is biased by R6 and R7. R10 provides a small amount of attenuation that counteracts the small voltage gain through the delay line.

VR1 forms a simple mixer circuit which combines the outputs of the last two stages of IC1, and this component is adjusted to produce maximum cancelling of the clock signal. C6 provides a certain amount of filtering at the output in addition to that produced by the main filter circuit.

The mixer stage is a conventional operational amplifier summing mode circuit which utilises IC2. C12 rolls off the high frequency response of the mixer stage slightly and gives a small amount of additional output filtering. The effect can be switched out by opening S2 to cut the delayed signal to the mixer.

OSCILLATORS

Fig. 3 shows the circuit diagram of the sweep and clock oscillators, together with the supply and regulator circuitry.

The clock oscillator uses the four two input NOR gates of a 4001 CMOS device, and all four gates have their two inputs connected together so that they act as four inverters.

R.A. Penfold

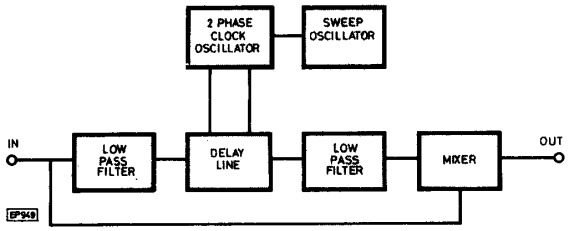


Fig. 1. Block diagram of Mini Chorus Unit

IC4a and IC4b are used in a conventional CMOS astable circuit, and IC4c is used as a buffer stage at the output of the oscillator. IC4d is used as an inverter which gives an output signal which is complementary to that at the output of IC4c, and thus gives the required two phase clock signal.

The frequency of this type of astable can be varied by applying a control voltage to the input of the first inverter via a series resistor (R24). TR3 is used as a buffer stage between the sweep and clock oscillators and is needed in order to present a suitably high load impedance to the sweep oscillator.

The sweep oscillator uses operational amplifier IC3 in a well known configuration, and this oscillator operates by charging and discharging C14 through VR2, R22, and the output stage of IC3. C14 charges and discharges exponentially and a non-linear triangular waveform is therefore produced across C14, and this signal is used to sweep the clock oscillator up and down in frequency. VR2 gives an adjustable frequency range of approximately 0·1Hz to nearly 10Hz.

The circuit requires a reasonably stable 15 volt supply, and this is derived from two 9 volt batteries in series using a simple series regulator circuit which consists of TR4, R26, D1, D2, and C17. This uses a well known configuration with the Zener stabiliser formed by R26, D1, and D2 being used to drive emitter follower transistor TR4. D2 is used to boost the input voltage to TR4 by about 0·65 volts to compensate for the voltage drop of approximately the same amount between the base and emitter of TR4.

The current consumption of the circuit is about 11ma and this gives a reasonable battery life using PP3s or equivalents, but if the unit is likely to receive a great deal of use it would probably be more economic to use larger batteries or rechargeable nickel-cadmium types.

CONSTRUCTION

The printed circuit board design is shown in Fig. 4 and the wiring of the unit is illustrated in Fig. 5.

IC1 and IC4 are both MOS devices, and while the 4001 integrated circuit costs only a few pence, the SAD1024A is quite expensive and should be treated with respect. Use a socket for this component and do not fit it into place until the printed circuit board is in other respects complete. Leave it in its protective packaging until it is to be plugged into circuit, and try to avoid touching the pins.

All the components, including PP3 size batteries, can be fitted into a diecast aluminium box having approximate outside dimensions of 150 by 80 by 50mm. A diecast aluminium box is ideal for this application as it is both very strong and has excellent screening properties. S2 is mounted centrally on the top panel of the case so that it can be

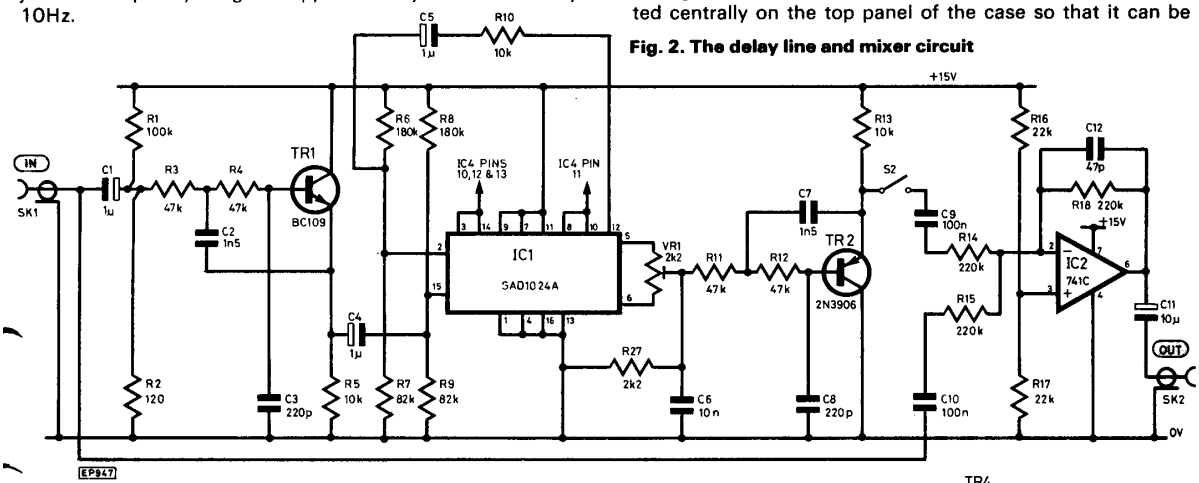


Fig. 2. The delay line and mixer circuit

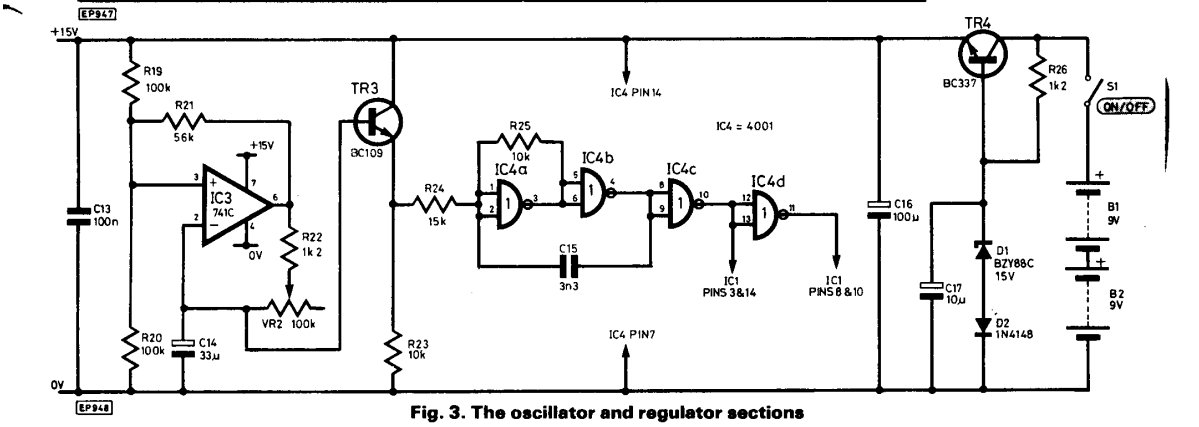


Fig. 3. The oscillator and regulator sections

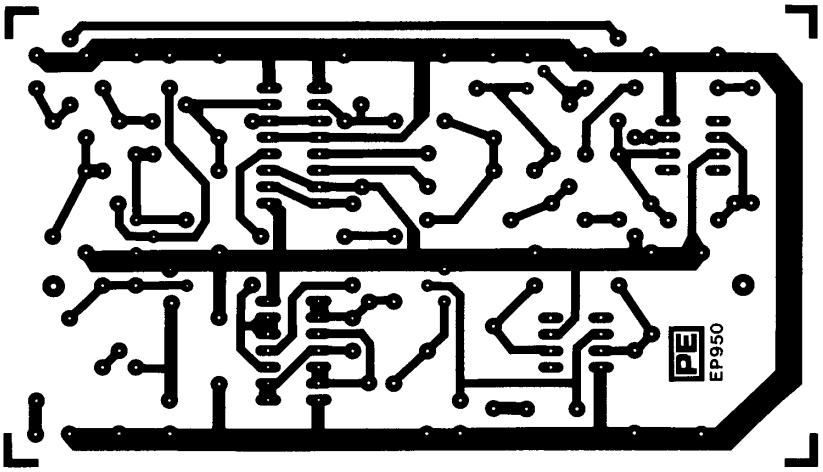


Fig. 4. Printed circuit

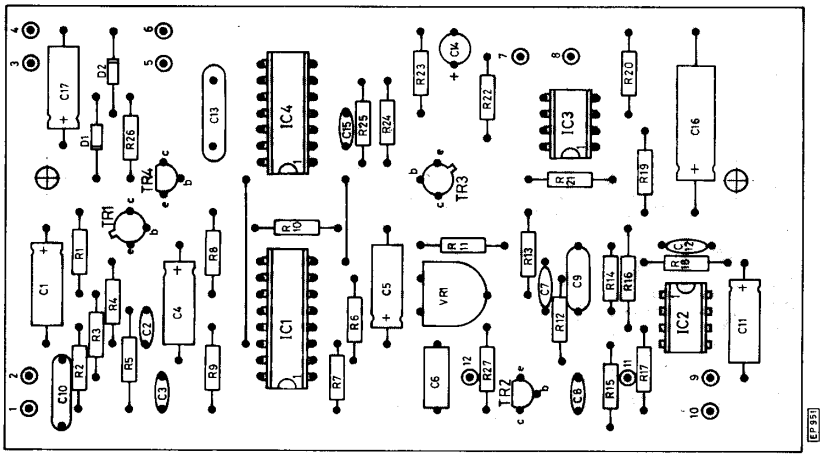
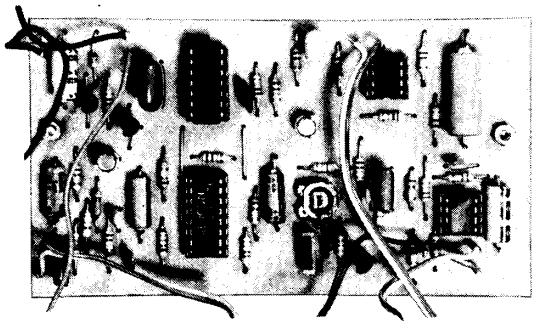
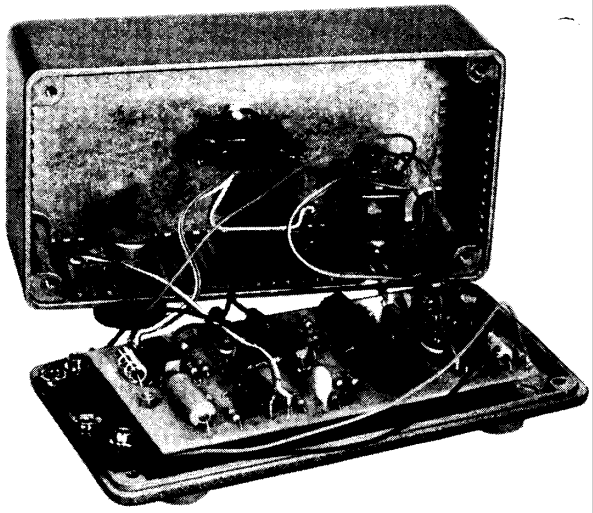


Fig. 5. Board assembly

operated by foot. SK1, SK2, and VR2 are mounted along one of the 150 by 50mm sides and must be offset slightly towards the top so that sufficient room is left for the printed circuit board. The latter is mounted on the removable base panel of the case. S2 is a pair of make contacts on the input socket SK1, so that the unit is automatically switched on and off when the input is connected to and disconnected from SK1 (which is standard practice with effects units). A separate on/off switch can obviously be employed if preferred.





COMPONENTS

Resistors

R1,19,20	100k	(3 off)
R2	120k	
R3,4,11,12	47k	(4 off)
R5,10,13,23,25	10k	(5 off)
R6,8	180k	(2 off)
R7,9	82k	(2 off)
R14,15,18	220k	(3 off)
R16,17	22k	(2 off)
R21	56k	
R22,26	1k2	(2 off)
R24	15k	
R27	2k2	

All resistors ¼W 5%

Capacitors

C1,4,5	1µ 63V elect (3 off)
C2,7	1n5 ceramic 10% (2 off)
C3,8	220p ceramic 10% (2 off)
C6	10n carbonate
C9,10,13	100n polyester
C11,17	10µ 25V elect (2 off)
C12	47p ceramic 10%
C14	33µ tantalum
C15	3n3 ceramic 10%
C16	100µ 25V elect

Semiconductors

D1	BZY88C15V (15V 400mW Zener)	
D2	1N4148	
IC1	SAD1024A	
IC2,3	741C	(2 off)
IC4	4001	
TR1,3	BC109	(2 off)
TR2	2N3906	
TR4	BC337	

Potentiometers

VR1	2k2 0·1W horizontal preset
VR2	100k linear carbon

Miscellaneous

SK1/S1 Standard jack with DPDT contacts (Maplin)
SK2 Standard jack
S2 Heavy duty push-to-make, push-to-break type
B1, 2 PP3 size 9 volt (2 off)
Battery connectors
Control knob
Printed circuit board
One 16 pin DIL, one 14 pin DIL, and two 8 pin DIL i.c. sockets
Veropins
6BA fixings
Diecast aluminium box about 150 x 80 x 50mm
Wire, solder, etc.

It is advisable to fix four cabinet feet to the base of the unit so that it does not tend to slip away when S2 is operated.

ADJUSTMENT

Only one preset needs to be adjusted before the unit is ready for use, and this is VR1. If an oscilloscope or a.c. millivoltmeter is available, this can be used to monitor the signal at the wiper terminal of VR1 while this component is adjusted for minimum signal level. There should be no input signal present when making this adjustment. A simple alternative which does not require any test equipment is to add a capacitor of around 47nF in parallel with C15 so that the clock oscillator operates at an audible frequency. VR1 is then adjusted for minimum output of the clock tone.

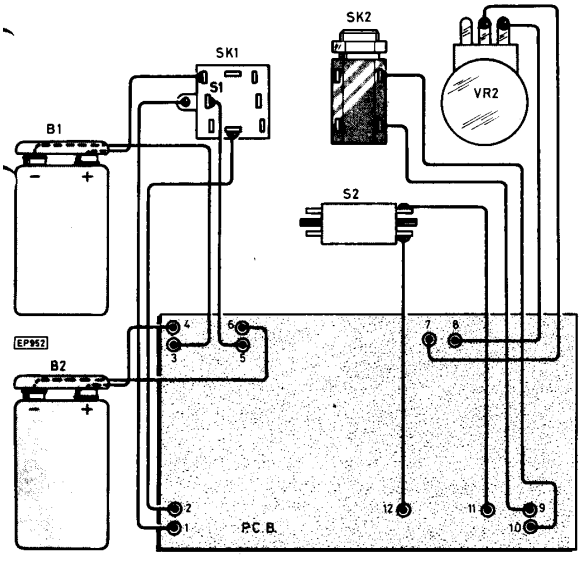
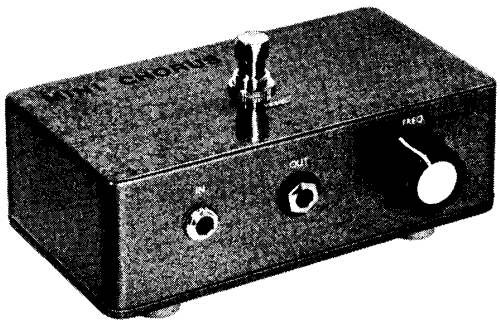


Fig. 6. External component connections to board



The completed unit

INPUT LEVEL

The output noise level of the unit is well below 1mV r.m.s., and provided an input signal level of at least a few hundred millivolts r.m.s. is used a signal to noise ratio of about 60dB or more will be obtained. An input level of up to about 1 volt r.m.s. can be handled by the circuit without serious distortion occurring. ★