OnChip Systems

PD 508
Octal Sample & Hold

PRODUCT HIGHLIGHTS

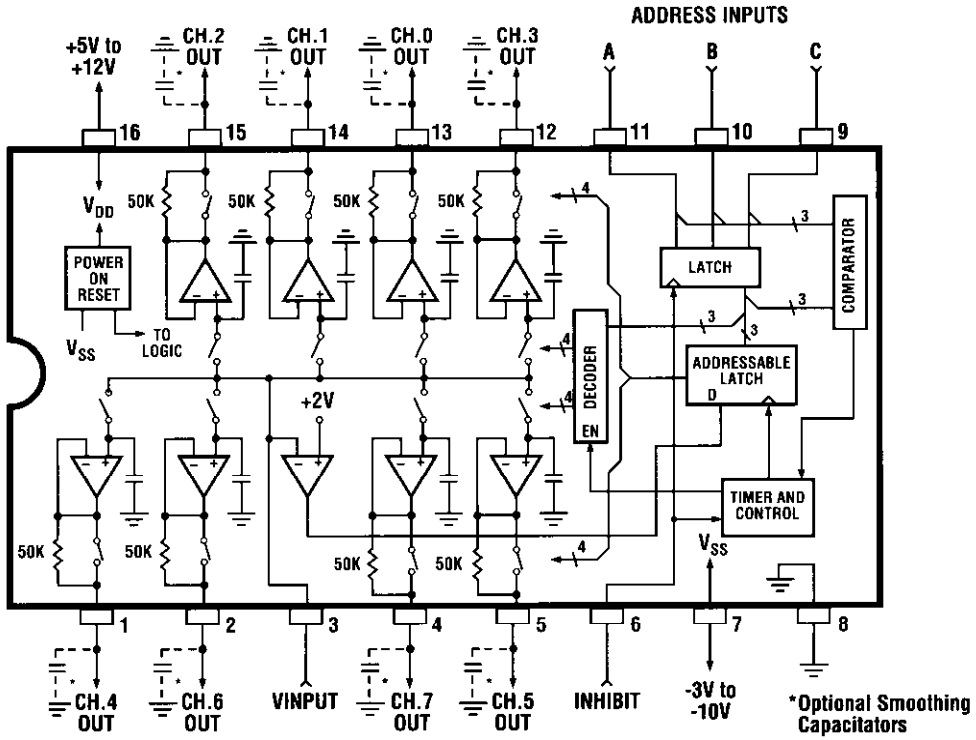
- 8 Matched Sample and Holds in a Single Package
- Excellent Linearity and Accuracy
- Fast Acquisition Time: to 12 Bits in Less Than 2.5us
- Low Hold Step: <2 mV
- Low Droop Rate: <1 mV/ms
- Internal Hold Capacitors
- Supply Independent TTL/CMOS Compatible Inputs
- Pin Compatible with CD4051
- Easy to Use
- Low Cost

APPLICATIONS:

- Multi-channel Data Acquisition Systems
- Automatic Test Equipment
- Digital Audio Systems
- Robotics & Industrial Control
- Instrumentation
- Event Analysis
- Software Trimming and Calibration
- Multiple Waveform Generation

ORDERING INFORMATION:

PART NUMBER	PACKAGE TYPE	TEMP RANGE
PD 508P	16 pin PDIP	0°C to +70°C
PD 508C	16 pin CDIP	-20°C to +85°C
PD 508S	16 pin SOIC	0°C to +70°C



PD 508 Block Diagram and Typical Connection

DESCRIPTION

The PD 508 is an 8 channel multiplexed Sample and Hold intended for generating multiple programmable voltages. Containing an analog multiplexer, 3 bit decoder, and 8 individual Sample and Holds, the 508 can acquire a voltage into any one of its 8 outputs to within 0.05% in less than 2.5us.

Pin-for-pin compatible with industry standard CD4051 CMOS multiplexer, the PD 508 additionally contains many enhanced features over other multiplexed Sample and Holds. An on-board 3-bit latch and timing generator (one-shot) greatly simplify interface to a microprocessor system, while still maintaining compatibility as a replacement part in existing systems. In addition, each channel offers individually selectable low (<200 ohm) or high (50K nominal) output impedance for implementing dual time constant smoothing filters at each output. Such a feature allows software generated control waveforms to have both fast transitions and low ripple.

With true push-pull outputs able to swing within 2.5 volts of either supply, each channel also delivers high performance in offset and hold step size. Ease of use is further enhanced with outputs which can handle any amount of capacitance with no degradation in performance, and CMOS logic inputs which are TTL compatible regardless of supplies.

Complete with all hold and timing capacitors on-chip and requiring no external components, the PD 508 makes interface between microprocessor and voltage controlled devices exceptionally simple and economical.

SPECIFICATIONS

V_{DD} = +8V V_{SS} = -5V T_A = +20°C

Parameter	Min.	Typical	Max	Units
T_{ACQ}, Acquisition Time[1]	—	2	—	µs
Acquisition Error	—	0.01	0.03	%
t_{APR}, Aperture Time[2]	—	2.5	—	µs
Aperture Jitter	—	250	600	ns
t_{AS}, Address Set-up Time	—	—	100	ns
t_{AH}, Address Hold Time	—	—	300	ns
t_{IW}, Inhibit Low Time	200	—	—	ns
Input/Output Voltage Range	V_{SS} + 2.5	—	V_{DD} - 2.0	V
Linearity	—	0.05	—	%
Input Bias Current	—	—	1	nA
Input Capacitance	—	2	—	pF
Input Feedthrough	—	2	—	mV
Input/Output Offset[3]	—	± 10	—	mV
Hold Step	—	2	—	mV
Hold Droop	—	0.2	1	mV/ms
Channel Crosstalk[4]	-60	—	—	dB
Digital Noise Leakage[5]	—	2	—	mV RMS
Output Slew Rate[6]	—	3	—	V/us
Output Sourcing Impedance	—	200	—	ohm
Output Sinking Impedance[7]	—	500	—	ohm
Output Source Drive	—	3	—	mA
Output Sink Drive[7]	—	2.4	—	mA
Logic Low Level	—	—	0.8	V
Logic High Level	2.4	—	—	V
Logic Input Current	—	—	1	µA
Max Logic Swings	V_{SS}	—	V_{DD}	V
Supply Voltage, V_{DD} - V_{SS}	9	—	16	V
Supply Current	—	3	—	mA

Notes:
1) Determined by an internal timer.
2) Includes internally generated sample command time and delay time from INHIBIT falling edge.
3) While channel is sampling. V_O = 0V.
4) Between adjacent channels. Crosstalk is lower between non-adjacent channels.
5) Digital noise consists mostly of narrow spikes coincident with input logic level transitions.
6) No load capacitance.
7) V_{SS} - V_O = 5V.

APPLICATION HINTS

Power Supplies

As long as the maximum supply voltage between V_{DD} (pin 16) and V_{SS} (pin 7) is not allowed to exceed 16V, then the positive supply (V_{DD}) may be any voltage from +4.5V to +12.5V, while the negative supply may range from -2.5V to -10.5V. The values selected for the supplies determine the maximum input and output voltage excursions before significant gain errors occur (distortion): The input/outputs may swing to within 2.0 volts of the positive supply, and within 2.5 volts of the negative supply. Thus, ± 8V supplies will accommodate inputs and outputs between +5V and -5V, while ± 5V supplies will allow swings up to ± 2.5 volts. Supplies need not be symmetrical: For a 0 to +5V output, +8 and -3 to -6V supplies maybe used, while a 0 to +10V output will require a +12,-3V supply.

The threshold levels of all logic inputs are TTL compatible and unaffected by either supply.

Basic Operation and Timing

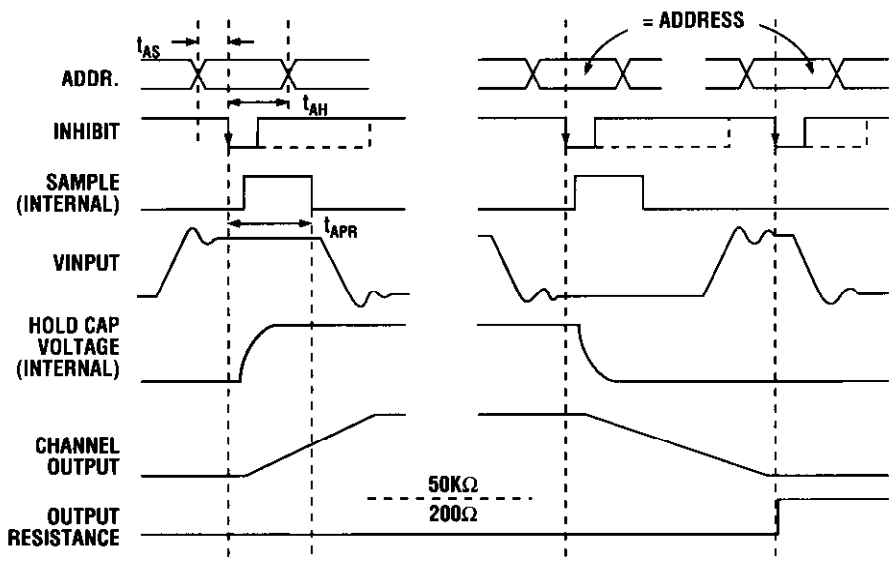
The PD 508 operates in essentially two basic modes of operation: one for updating (refreshing) the 8 Sample & Holds, and the other for switching in or out the 50K ohm resistor in each channel output. The timing for both modes are shown in Figure 1.

The basic update cycle begins with the input voltage (normally from a DAC) and the three address inputs changing to their new value. The order in which these occur does not matter, as long as the voltage has settled to its proper value (at least most of the way) and the address inputs are stable at least t_{AS} prior to the INHIBIT signal falling low. The falling edge of INHIBIT then begins the sampling sequence: Firstly, the address is latched into the 3 bit address latch; after a short delay (approx. 200nS) to allow for decoder settling, the internal timer (one shot) triggers and closes the selected

Sample and Hold switch for nominally 2uS. After this period, the switch reopens regardless of when INHIBIT returns high; in fact, the only requirement for the INHIBIT pulse is that it remain low a minimum of t_{IW} (200nS). Finally, after the switch reopens, the input voltage may change; since the sample command is internal, the aperture time, t_{APR}, must be taken from the INHIBIT falling edge, and the input should remain at its proper value for at least this period.

As can be seen, the timing requirements are quite flexible. Since the address inputs are latched on the negative edge of INHIBIT, they may change any time, t_{AH} (300nS), after being latched. The address inputs can therefore connect directly to the microprocessor address/data bus, allowing the microprocessor to load new data into the DAC, load the new address into the 508, and move on to other tasks while the 508 selected channel is acquiring the DAC voltage. Of course, the device may still be used in existing systems where the INHIBIT low time determines the sampling period and where INHIBIT must return high before the address changes.

It should be noted that the channel output voltage followers are slower than the charging times of the Sample & Hold capacitors, especially when loaded with external capacitance. Thus, the channels are actually acquiring the input voltage to within 0.05% in the allotted 2uS, even



PD 508 Timing Diagram

though the outputs may take milliseconds to slew to their final value.

Changing the value of output resistance is accomplished in a similar manner to updating the Sample & Holds. In fact, the only way in which the 508 distinguishes between the two operations is by the contents of the address latches: If the new address strobed into the latch is different from the previous address in the latch, then the selected Sample & Holds will be updated as previously explained; if the new address is the same as the previous address, however, then the output resistance of the selected channel will be set according to the input voltage, and none of the Sample & Holds will be affected. An input voltage less than +2 volts will cause the output resistance to take on its low value (essentially that of the switch, or about 200 ohm), while an input greater than +2V will result in the 50K ohm output resistor being selected. The input voltage for this mode of operation may be either generated by the DAC output, or a separate logic output switched to the 508 input in place of the DAC output.

Note that the 508 also contains a power-on reset circuit which sets all outputs to their low resistance state upon power-up; this feature again allows this device to be used in existing and new systems which do not require the 508's selectable output resistance capability.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{EE}	16V
Voltage at any pin	V_{DD} + 0.3 V to V_{SS} - 0.3V
Current through any pin	± 50mA
Operating Temperature Range	0°C to 70°C, -20°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	300°C
Power Dissipation	500 mW

Input & Output Considerations

For best performance, the voltage input (pin 3) should be driven from a low impedance source, such as an op amp output. In addition, a small capacitor (e.g. 100-1000pF) from the op amp output back to the inverting input should be used to keep the output impedance low even at high frequencies.

To prevent possible latch-up, the input voltage should be restricted at all times and under all conditions to within the V_{DD} and V_{SS} supplies. If the supplies to the driving op amp are larger than those to the 508, then there exists the possibility of the op amp output being outside the 508 supplies, and some means, such as signal or Zener diodes in the feedback loop, should be added to ensure this condition can never occur.

Each channel output can source up to 3mA steady state for any positive supply. The output sink capability, however, is dependent on the difference between the most negative output voltage excursion and the negative supply, according to the following:

$$I_{OSINK}\ (mA) = 0.15\ (V_{SS} - V_O + 1)^2$$

Thus, for an output of V_O = -2.5V with V_{SS} = -5V, the maximum sink current is 330 uA (minimum load of 7.5K to ground); but for an output of 0V with V_{SS} = -5V, the maximum sink current rises to 2.4mA. (Of course, driving a load to ground with a minimum output of 0V requires no sink capability.)

The source and sink capability is especially important when the output is required to drive a large capacitive load, as this to a large extent determines the output charge rate when the low resistance state is selected: The equivalent output resistance in the sourcing condition is several hundred ohms, while in the sinking condition, the equivalent output resistance is 500-1000 ohms, depending on the minimum V_O-V_{SS} differential.

For load capacitance values greater than 1nF, the transient currents generated in the output stage can become much larger than the recommended 5mA limit; thus for these larger values, a 1K current limiting resistor should be placed between output and load capacitor.

The value of load capacitor, of course, is selected to give the desired time constant when the 50K nominal output resistor is selected. A 0.1uF, for instance, will allow the smoothing filter time constant to be selectable between 5mS and approximately 0.15mS.

In applications utilizing the selectable output resistance feature, the filtered output of the 508 may require buffering by an op amp voltage follower should the load impedance be too low. However, in many applications the input voltage port of the device to be controlled has high enough input impedance that it may be directly driven by the 508 outputs even in the high output impedance mode.

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