MN3105

CMOS Clock Generator/Driver for Ultra Low Voltage Operation BBD MN3300 Series

■ Overview

The MN3105 is a CMOS LSI generating two phase clock signal of low output impedance necessary to drive MN3300 series low voltage operation BBD.

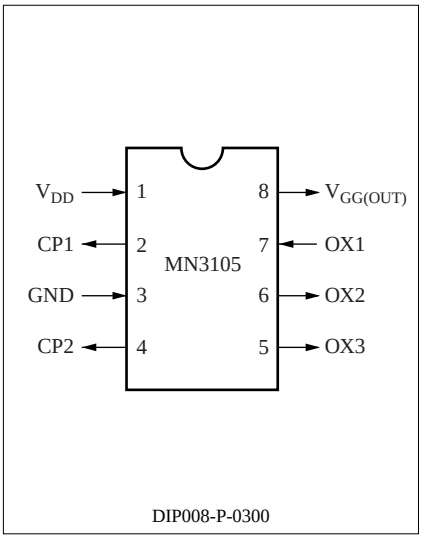
Self-excited oscillation is enabled by external capacitors and resistors and oscillation drive is possible by the separately-excited oscillation.

Clock signal frequency is 1/2 of oscillation frequency.

■ Features

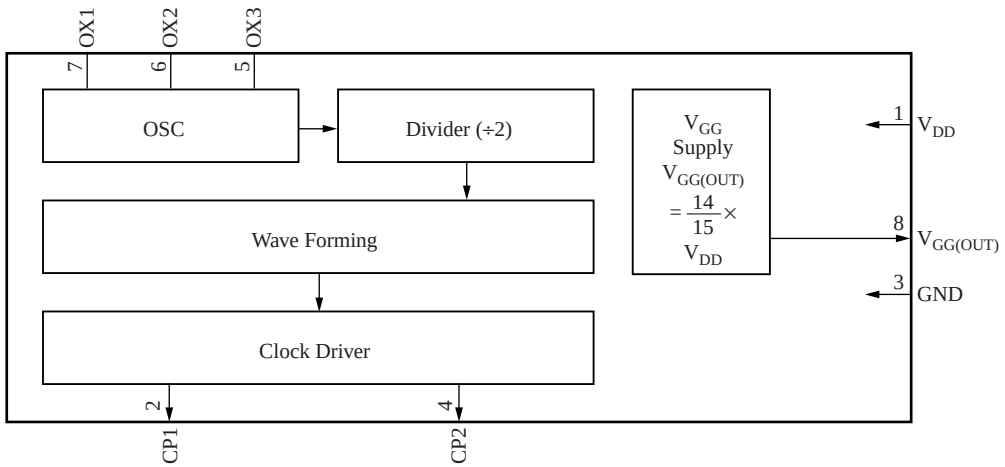
- Direct driving capability to 4096-stage ultra low voltage BBD.
- Self-excited oscillation and separate excitation drive are enabled.
- Two phase clock (Duty : 1/2) output.
- Single power supply : 1.8 to 5.0 V
- 8-Pin Dual-In-Line Plastic Package

■ Pin Assignment



DIP008-P-0300

■ Block Diagram



■ Absolute Maximum Ratings Ta=25°C

Parameter	Symbol	Ratings	Unit
Supply voltage*	V_{DD}	− 0.3 to +6.0	V
Input pin voltage*	V_I	− 0.3 to V_{DD}+0.3	V
Output pin voltage*	V_O	− 0.3 to V_{DD}+0.3	V
Power dissipation	P_D	200	mW
Operating ambient temperature	T_{opr}	−20 to +70	°C
Storage temperature	T_{stg}	−30 to +125	°C

Note) * : GND=0V

■ Operating Conditions Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}	GND=0V	+1.8	+3.0	+5.0	V

■ Electrical Characteristics Ta=25°C

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current	I_{DD}	No load		0.36		mA
Total power consumption	P_{tot}	Clock output 40 kHz		1.08		mW
OX1 input pin						
Input voltage "H" level	V_{IH}		$2/3V_{DD}$		V_{DD}	V
Input voltage "L" level	V_{IL}		0		$1/3V_{DD}$	V
Input leakage current	I_{LK}	V_I=0 to V_{DD}			30	µA
OX2 output pin						
Output current "H" level	I_{OH1}	V_O=2 V	0.3			mA
Output current "L" level	I_{OL1}	V_O=1 V	0.3			mA
Output leakage current	I_{LOL1}	V_{DD}=5 V, V_O=GND			30	µA
	I_{LOH1}	V_{DD}=5 V, V_O=V_{DD}			30	µA
OX3 output pin						
Output current "H" level	I_{OH2}	V_O=2 V	0.4			mA
Output current "L" level	I_{OL2}	V_O=1 V	0.8			mA
Output leakage current	I_{LOL2}	V_{DD}=5 V, V_O=GND			30	µA
	I_{LOH2}	V_{DD}=5 V, V_O=V_{DD}			30	µA
CP1 and CP2 output pins						
Output current "H" level	I_{OH3}	V_O=2 V	4			mA
Output current "L" level	I_{OL3}	V_O=1 V	4			mA
Output leakage current	I_{LOL3}	V_{DD}=5 V, V_O=GND			30	µA
	I_{LOH3}	V_{DD}=5 V, V_O=V_{DD}			30	µA
$V_{GG(OUT)}$ output pin*						
Output voltage	$V_{GG(OUT)}$			2.8		V

Note) * : This pin generates V_{GG} voltage exclusively applied for low voltage operation BBDs manufactured by us. Therefore, sometimes it might not besuitable for the application other than V_{GG} voltage of our BBDs. $V_{GG(OUT)}$ changes in the following formula depending on the value of VDD.

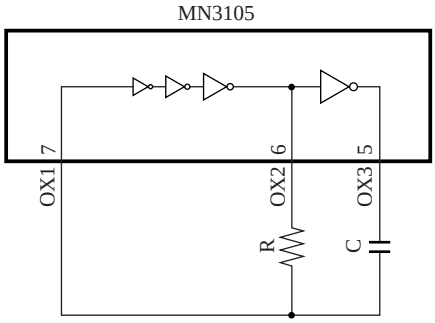
$$V_{GG(OUT)} \approx \frac{14}{15} V_{DD}$$

In case of driving the MN3300 series BBDs, should not use the $V_{GG(OUT)}$ pin.

■ Pin Descriptions

Pin No.	Symbol	Pin Name	Description	
1	V_{DD}	Supply voltage	Supply voltage of +3 V is applied.	
2	CP1	Clock output 1	The pin outputs a clock signal which has a duty of 1/2 and a frequency of 1/2 oscillation frequency, with the relation of negative phase to CP2.	
3	GND	Ground	Connected to ground.	
4	CP2	Clock output 2	Outputs a clock signal with the negative phase to CP1.	
5	OX3	C-R connection	In case of self-excited oscillation, C and R are connected. (Refer to the example of oscillation circuit.)	In case of separately-excited oscillation, OX2 and OX3 should be opened. OX1 is set to OSC input.
6	OX2			
7	OX1			
8	$V_{GG(OUT)}$	V_{GG} voltage output	2.8 V is output. (at V_{DD}=3 V), $V_{GG(OUT)}$=(14/15)V_{DD}	

■ Example of Oscillation Circuit



Oscillation circuit of the MN3105 is composed of 4-stage inverter and oscillation frequency is defined by the C-R time constant.
Following is an example of C, R.
Figure 1 shows f_{CP}*1-R characteristics.

Example \ Constant	R(Ω)	C(pF)	f_{OSC}(kHz)*2	f_{CP}(kHz)*1
Example 1	2k to 1M	22	20 to 2000	10 to 1000
Example 2	2k to 1M	100	5.2 to 960	2.6 to 480
Example 3	2k to 800k	330	2.0 to 360	1.0 to 180

Note) *1 : Clock frequency output from CP1 or CP2 pin.
*2 : Oscillation frequency of OX1, OX2 and OX3.

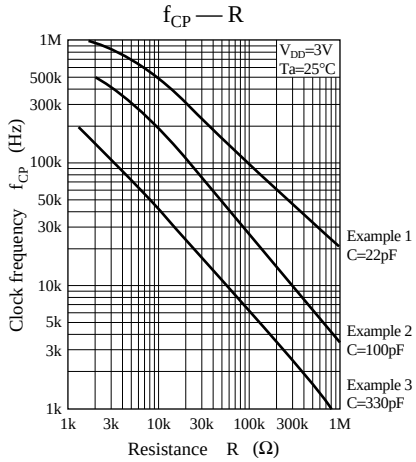
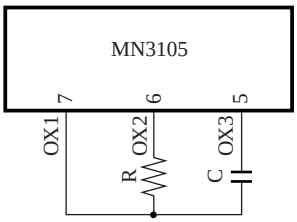


Fig.1 Example of Clock Oscillation Frequency Characteristics



■ Maximum Clock Frequency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption. The maximum power dissipation for this LSI, P_D, is 200 mW.

If the clock frequency or the load capacitance is increased, the power consumption will be increased. (Refer to Fig.2) Accordingly, in order to use the MN3105 with dissipation less than the P_D value, it is necessary to select adequate values for the clock frequency and load capacitance.

If V_{DD} is 5 V or less, the dissipation will not exceed the P_D value. (Provided that the BBD equivalent to 4096 stages or less is used.)

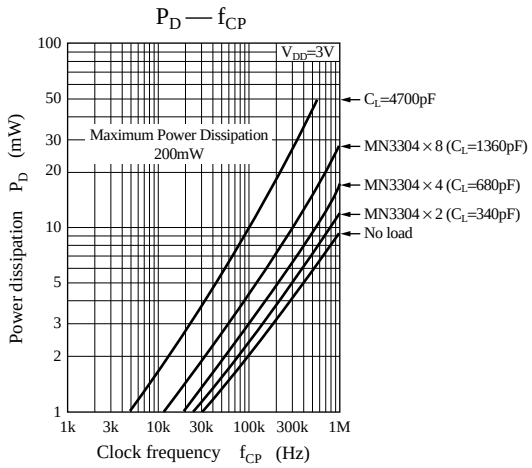


Fig.2 Example of Power Dissipation vs Clock Frequency

■ Package Dimensions (Unit : mm)

• DIP008-P-0300