SOLID STATE REVERB UNIT

Where have all the spring lines gone? Gone to lesser projects in other magazines, that's where. Meanwhile we present this cheap, simple, but high-quality unit using solid state technology.

Design by Charles Blakey.



t last — a reverberation unit which is not a pseudo echo effect and does not suffer from the defects of spring line devices. The unit described below will interface with virtually any preamplified signal and is ideal for direct use with most musical instruments or for incorporating in the 'echo-send' line of mixers. The design has been made possible by a new 3328-stage bucket brigade device having six tapped delays and capable of producing a useful reverberation time of about three seconds.

Sound emitted in an enclosed space will be subjected to both simple and multiple reflections from internal surfaces. Since these surfaces are at varying distances, the time for these reflections to occur and then decay by absorption will vary. The effect is a build-up of sound known as reverberation. When playing a musical instrument in the home, small studio or some other venue, the decay time can be very small coupled with a high absorption loss; the result is a weak sound when compared to recorded music or to live music played in a large hall

Until now the only low-cost method of simulating acoustic reverberation has been the use of spring lines. These units, however, are prone to vibration, require a high

power consumption for effective driving and are prone to producing distorted resonant peaks. Furthermore it is not possible to adjust the reverberation time and in many instances a short reverberation can be very effective. Another option has been available for some years, namely, the use of bucket brigade devices to electronically delay signals. While claims have been made for reverberation effects based on these products, a realistic unit would require at least three dual 512-stage BBDs, such as the Reticon SAD1024A. The cost and complexity of the latter approach puts it beyond the reach of the average constructor.

Beyond The Pail

The reverberation unit utilises the MN3011, which is the latest in a series of bucket brigade devices for audio applications to come from National Panasonic. They are all fabricated in PMOS and for a start you can forget most of what you may have read about the disadvantages of PMOS BBDs. It is a fact that they are somewhat limited in clocking speed (10 kHz to 100 kHz) and also have a limited bandwidth, typically 10 to 12 kHz. The latter, however, is not usually a limitation since the bandwidth is often restricted

by the desire for long delay times. What makes the series ideal for audio applications is their low insertion loss, low distortion and excellent signal-to-noise ratio and for the MN3011 the specified values are 0 dB, 0.4% and 76 dB respectively.

The IC is unusual in that it has 12 pins but is the length of a normal 18-pin package; the functional block diagram and pinout for the MN3011 is shown in Fig. 1. As is normal with such devices it requires two power supplies, $V_{\rm DD}$ and $V_{\rm GG}$; the former may be up to -18 V with respect to ground while V_{GG} should be $\pm 1 \text{ V}$ higher than V_{DD} Bucket brigade, or charge coupled, devices are analogue shift registers which operate by sampling the input signal at a rate determined by an external clock. The signal level at the time of sampling is stored on an internal capacitor; this charge is then clocked down a series of capacitors by means of internal switches. The transfer process is accomplished by a dual clock whose outputs are in antiphase and so are alternately opening and closing adjacent switches. It will be apparent that the slower the clock speed the longer the delay. Since the devices operate at high clocking speeds the input signals are faithfully reproduced at the output.

The most interesting feature of the V

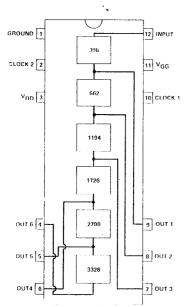


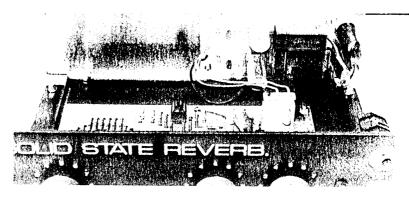
Fig. 1 Pinout and internal layout of the MN3011. The centre three pins on each side of this 18 pin package are absent

MN3011 is that it has six tapped delays and Fig. 1 shows the number of stages for each tapping. The tappings are not evenly spaced since otherwise the reverberant sound would have a distinct flutter. If the device was being clocked at 10 kHz then the delays from outputs one to six would be 19.8, 33.1, 59.7, 86.3, 139.5 and 166.4 milliseconds respectively. If these delay times are mutiplied by 0.33 then one obtains the equivaler t room path length for one trip, ie the longest delay is equal to a room length of 55 metres (181 feet). Reverberation time is usually measured as the time taken for the power to decay to one millionth of its initial level (60 dB down). For the present design the time was measured for the output level to fall to one hundredth of its initial level (-40 dB) and at the longest delay this was found to be about three seconds

Blocks 'n Clocks

The block diagram of the circuit for the reverberation unit is shown in Fig. 2. First there is the dual clock driver, which is another National Panasonic device, the MN3101. It has an oscillator, divider and wave form shaping and produces the dual clock pulses required by the MN3011. It reduces component count and is lower in cost than other alternatives, such as a 4007. A further advantage is that it also generates the required V_{CC} voltage.

The unit will operate satisfactorily



with any input signal greater than 280 mV RMS and higher input signals are attenuated by the input potentiometer. The signal is also reduced by half in amplifier A1 and inputs higher than 140 mV to the first filter are indicated by a LED peak detector circuit. Although the MN3011 will accept signal levels up to 780 mV before the distortion value stated earlier is exceeded, it will become apparent that the effect of reverberation can lead to reinforcement of signals and consequently this has to be allowed for. The only preset in the circuit is used to apply a bias voltage to the signal. The precise value of this voltage is not very critical in the current design and the object is to keep the signal at a level where it will not be distorted or clipped within the BBD.

The main problem with BBDs is the inability to completely cancel out the clock pulses and these can form audible cross products with the input signal. In order to prevent this foldover distortion, the bandwidth of the input signal should be limited to between a half and a third of the clock frequency. Filter F1 in Fig. 2 is a lowpass filter with a cut-off frequency of 3.6 kHz. This may seem rather low but in fact it is equivalent to the upper reverberation limit of most spring lines and the BBD scores in respect of low frequency responses since springs usually give rise

to 'booming' below 100 Hz. The limited bandwidth is compensated by mixing the original signal with the reverberated signal at the output stage. The filtered signal goes to the MN3011 and the six output stages are summed to give a composite signal with different delay times. This signal is again filtered with a lowpass filter with a cut-off frequency of 3.6 kHz, to remove residual clock glitches, prior to mixing with the original signal at the output amplifier. A2.

The most important feature, however, is that the signal from the longest delay is returned, slightly attenuated, to the input and subjected to further delays. This is the reverberation effect and with the times given earlier the sound will simulate the effect of the first reaching a surface 55 metres away (assuming slowest clocking rate) and then being reflected back as well as being reflected from other surfaces closer than the 55 metre surface. The whole process is repeated until the original delayed signal and its reflections die away. In the meantime new signals are being recycled and the overall effect is a build-up of sound — reverberation.

Construction

The construction is very straightforward but the following precautions should be observed. First,

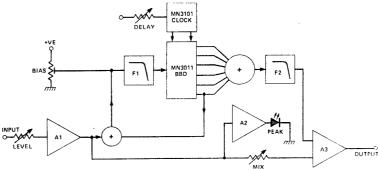


Fig. 2 Block diagram of the ETI Solid State Reverberation unit.

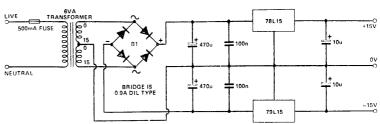


Fig. 4 Circuit diagram of a suitable PSU for this project.

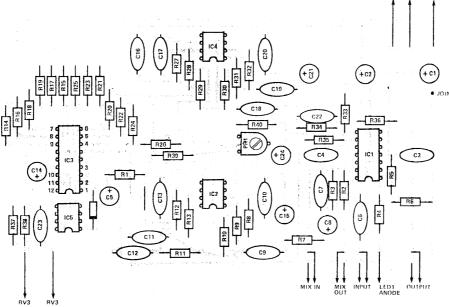


Fig. 3 Component overlay for the reverberation unit.

make sure you get the correct orientation of the ICs which are clearly shown on the component overlay. Second, the MN3011 is a CMOS device and with the advent of 'B' series devices we have all become rather careless as regards handling such ICs. For the MN3011, however, take the precaution of working on a grounded

PSU PARTS LIST.

	30 1/W13 E131		
Capacito	ors		
C1,2	470u 35 V PCB electrolytic		
C3.4	100n polyester		
C5,6	10u 35 V PCB electrolytic		
Semicon	ductors		
1C1	78L15		
IC2	79L15		
BR1	0A9 DIL type		
Miscella	neous		
	ee Buylines); PCB-mountin		
transform	mer (15-0-15, 6 VA); 500 mA main		
fuse and	chassis-mounting holder.		

PARTS LIST

TARIS LIST				
R1	¼ W 5% except where stated) 10R ½ W	PR1	47k miniature horizontal preset	
R2,5,7,9,				
13,32,33,39	100k	Capacitors	as assument a lat	
R3,34	51k	C1,2	10u 35 V PCB electrolytic	
R4	330R	C3,4	100n polyester	
R6	1k3	C 5	22u 35 V PCB electrolytic	
R8,12,27,31	33k	C.6	220n polyester	
R 10,29,37	47k	C7,10,13,	_	
R11, 30	56k	20,22	220p polystyrene	
R14,16,18,20,		C8,14,15,	,	
22,24	56k 1%	21,24	3u3 63 V PCB electrolytic	
R15	100k 1%	C9,11,12,		
R17	110k 1%	18,19	2n7 polystyrene	
R19	120k 1%	C16	2n2 polystyrene	
R21	130k 1%	C17	270p polystyrene	
R23	150k 1%	C23	33p polystyrene	
R25	160k 1%			
R26	200k	Semiconductors		
R28	82k	IC1	TL074	
R35	18k	IC2, 4	LM358	
R36	1k0	IC3	MN3011	
R38	36k	IC5	MN3101	
	68k	D1	1N4148	
R40	OOK	IED1	5 mm red LED	
Potentiometers		Miscellaneous		
		5K1.2	mono jack sockets	
RV1	100k logarithmic	PCB (see Buylines); IC sockets; case (Vero		
RV2	10k logarithmic	order no. 91-2673G).		
RV3	RV3 470k linear order no. 91-2673G).			

metal surface, such as a piece of aluminium foil, do not insert the IC with the power on and do not use a soldering iron on the PCB with the IC installed

The PCB supplied with the kit has a ground plane to reduce interference from and to other electronic equipment as well as to reduce noise. This feature allows greater freedom in locating the unit, eg it does not have to be housed in a separate metal case. A ground plane comprises a metallized surface on the component side except for small areas around the holes for the components. Ensure that the component leads do not touch the ground plane - which is not difficult and preferably solder the resistors and axial capacitors in place with a thin piece of card between the component and the board so that the former are not in physical contact with the ground plane. After soldering the card is removed. The latter step is not essential. The one wire link must be made with insulated wire. The ground plane has to be connected to the 0 V line and some 15 mm from where the latter is connected to the PCB there is a hole marked 'join'. A piece of wire should be placed through this hole and soldered on both sides of the PCB.

The PCB has been laid out such that the BBD and clock are as far away as practical from the signal input and output. This separation should be maintained if the unit is housed in a

box and all wiring should be kept as short and as neat as practical, with the audio connections being made with miniature screened cable.

The unit requires a ± 15 V power supply and the current consumption is a miserly 13 mA at \pm 15 V and 9 mA on the -15 V line. If a separate power supply is required then a suitable PSU is shown in Fig. 4. A PCB-mounted transformer is preferred, and it should be mounted as far away from the BBD as practical. The photographs show the unit inside a Vero 'G' range case with internal dimensions of approximately 218 x 138 x 50 mm.

HOW IT WORKS

The input signal is attenuated by RV1 and also by the inverting amplifier built around IC1a which has a gain of about 0.5. From IC1a the signal goes three ways. A comparator built around IC1b forms a peak

ICTa the signal goes three ways. A comparator built around ICTb forms a peak detector to indicate optimum signal level, while RV2 and R35 allow mixing of the original signal with the reverberated signal in the inverting amplifier configured around ICTc. The component values in this section are such that equal proportions of the two signals may be mixed. Finally the signal also passes to two active filters constructed around IC2 which have a 12 dB/octave roll-off for each stage and a cut-off frequency of 3.6 kHz.

From the above filter stages the signal passes into the MN3011 and the six delay outputs are summed by the resistor network formed by R14 to R25. Note that the shorter the delay, the less the attenuation. From the longest delay (pin 4) the signal goes via R25 back to the input of the filter and thus provides recycling of the delayed signal in order to generate a true reverberation effect. The reverberated signal is filtered by two active filters constructed around IC4 and these have the same characteristics as the input filters. Between the active filter stages some passive filters have also been

added to increase the roll-off; the loss in these filters is compensated by increasing the gain of the active filters.

The dual clock for the MN3011 is provided by IC5 and with the components shown, the clock frequency may be manually varied with RV3 over the range 10 kHz to 100 kHz, allowing maximum first pass delays from 16.64 to 166.4 milliseconds. Pin B of IC5 provides the V_{GC} voltage for the MN3011. Since both IC3 and IC5 are P-channel CMOS it would be normal to operate them from a -15 V supply. Voltages are, however, relative and by connecting +15 V to the ground pin and ground (0 V) to the V_{DD} pin they will operate happily with positive signal inputs. R1 and C5 prevent clocking signals getting back into the power lines. The filters are also operated from a single +15 V supply and this avoids any problems which may arise from excessive bipolar signals, ie they will be clipped at +15 V or ground and not damage the BBD. The bias voltage required by the BBD and the filters is primarily to allow them to accept bipolar signals; this voltage is provided by the resistive divider using components R39, PR1 and R40 and is applied to the non-inverting input of the filter op-amps. of the filter op-amps.

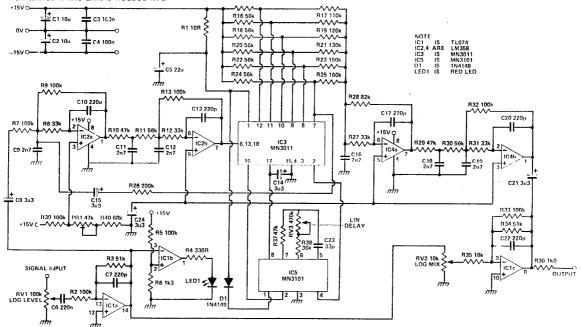
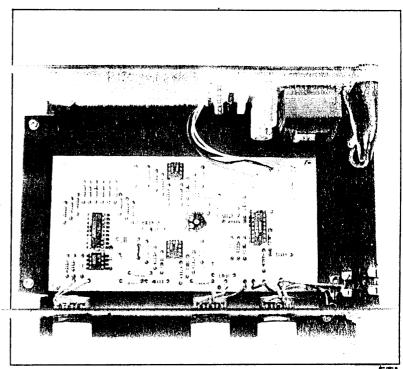


Fig. 5 Circuit diagram for the ETI Reverb.

Setting Up And Use

The only setting up required is adjustment of PR1. If a sinewave source is available then the latter may be used as the signal source and PR1 adjusted by ear, or with an oscilloscope, for minimum distortion. Alternatively measure the voltage at the junction of PR1 and R40 and adjust PR1 to give a reading of 6V2.

The unit has a signal-to-noise ratio of better than 60 dB but this requires that it is operated with the peak indicator LED just glowing or occasionally illuminating. The output level will vary from about 0V5 to 1 V RMS, depending on the amount of mixing of the original signal, and these levels should ensure adequate response from most amplifiers, mixers, and so on. In other words, by keeping input signals at maximum level the amplifier setting will be such that during periods of no signal the residual noise will not be obtrusive. This is common practice with recorders, many of which have much lower signal-to-noise ratios.



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ETI REVERB.