The SAD-512D is a general-purpose *S*ampled *A*nalog *D*elay device fabricated using N-channel silicon-gate technology in a bucket-brigade configuration to obtain flexible performance at low cost.

FEATURES

- 512-element delay
- On-chip driver requiring only single TTL-level clock input
- Clock-controlled delay: 0.2 sec to less than 200 μsec
- N-channel silicon-gate bucket-brigade technology
- Designed for self-cancellation of clocking modulation
- Wide signal-frequency range: 0 to more than 300 KHz
- Wide sampling clock frequency range: 1.5 KHz to more than 1.5 MHz
- Wide dynamic range: S/N > 70 dB
- Low distortion: less than 1%
- Single 15 volt power supply
- 8 pin mini DIP

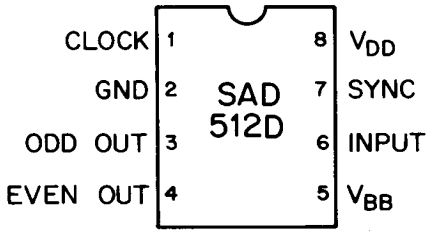

Figure 1. Pin Configuration.

TYPICAL APPLICATIONS

- Voice control of tape recorders
- Control of equalization filters
- Reverberation effects in stereo equipment
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Voice scrambling systems

DEVICE DESCRIPTION

The SAD-512D is a 512-element Bucket-Brigade Device (BBD) with internal clock drivers that require only a 5 volt (or higher) single-phase clock input.

The device has its output split into two channels to provide output over each full clock period in normal operation. The SAD-512D is manufactured using N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket-brigade charge-transfer device. It is packaged in a standard 8-lead dual-in-line package with pin configuration as shown in Fig. 1. The functional equivalent circuit is shown in Fig. 2. Several of the many applications are listed above.

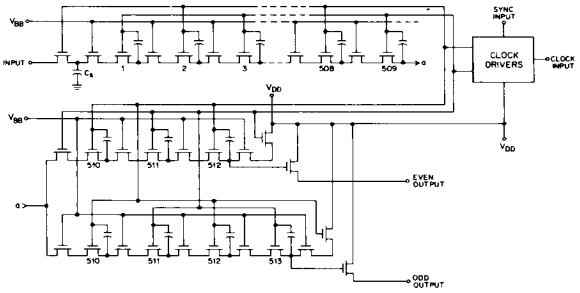

Figure 2. Equivalent Circuit-Diagram of SAD-512D.

CLOCK AND VOLTAGE REQUIREMENTS

Normal voltage levels and limits are given in the tabular specifications. Clock input is a rectangular wave which drives the on-chip clock drivers. The magnitude of the clock may be any positive pulse voltage from 5 volts to V_{DD}. The phase relationships of clock input, sync input (when used) and output waveforms are shown in Fig. 3. For convenience, V_{BB} may be biased to the same potential as V_{DD}. However, for optimum performance, it is recommended that V_{BB} be adjusted approximately one volt lower than V_{DD}.

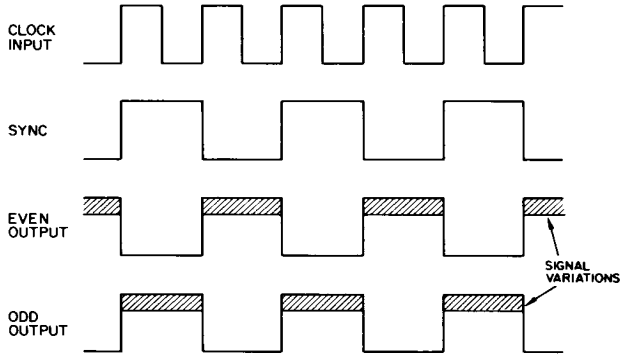

Figure 3. SAD-512D Clock Waveforms.

If the sync input is unused pin 7 should be connected to ground. If either output is unused it should be connected to V_{DD}.

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 f_S). Further, to recover a smooth delayed analog output a post filter having steep cutoff (e.g., 36 dB per octave or more) is desirable.

PERFORMANCE

Typical performance of the device is shown in the specifications and in the curves of Figs. 5–8. These data were obtained with the test configuration of Fig. 4. Internal dispersion becomes the limiting factor for sampling clock frequencies above 1.5 MHz.

Figures 5 and 6 indicate the linearity and show the rapid increase in distortion as the input level is increased toward

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saturation. For inputs less than approximately 500 millivolts rms the distortion is less than one percent. Between this point and the noise floor there is approximately 70 dB of dynamic range. This dynamic range assumes a 20 KHz audio filter and a sample rate of 100 KHz or faster. With a 20 KHz filter and 50 KHz sample rate the dynamic range is 63 dB. Broad-band dynamic range is better than 55 dB for all sample rates.

Figure 7 shows the loading effect of the output terminating resistor. The data indicates the output source followers have approximately 4000 ohms internal impedance. For this test each output was connected through a terminating resistor to ground, thus preventing any interaction between the two output followers.

Figure 8 shows the frequency response of the device when terminated as shown. The dotted lines indicate the range of variation from device to device.

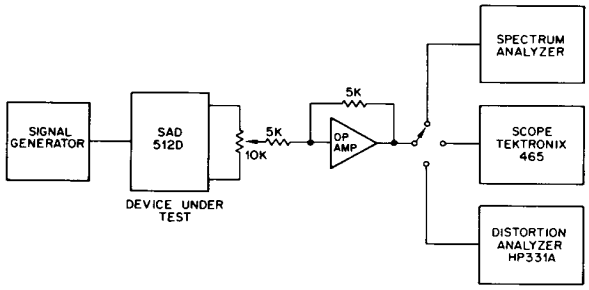

Figure 4. Test Set-up Used to Obtain the Data of Figures 5, 6, and 7.

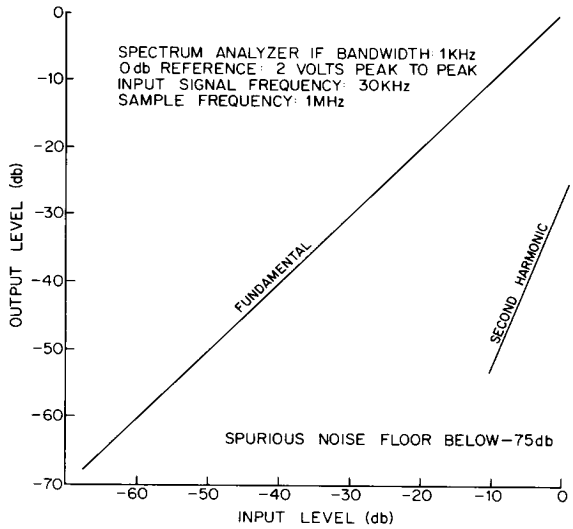

Figure 5. SAD-512D Transfer Characteristic.

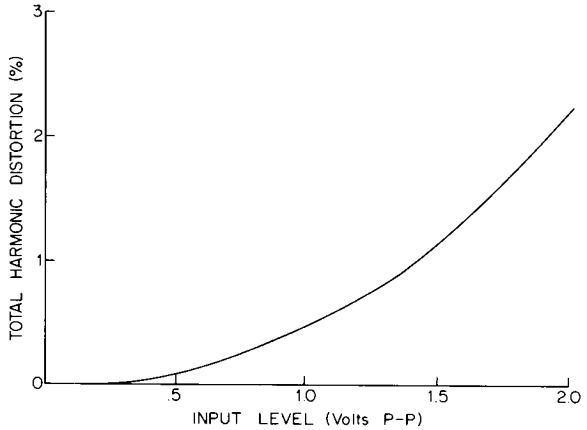

Figure 6. SAD-512D Distortion vs. Input Level.

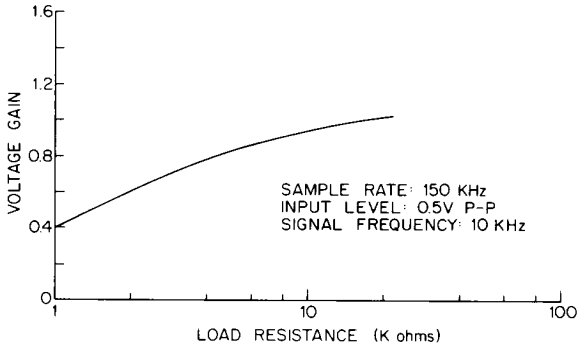

Figure 7. Dependence of Gain on Load Resistance.

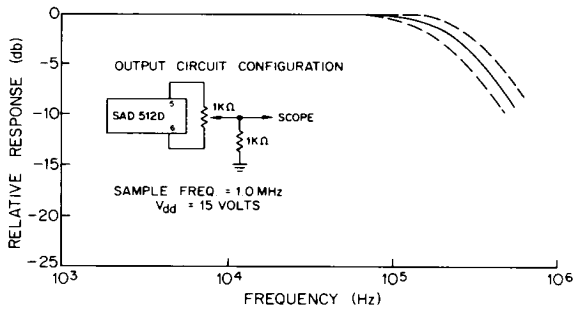

Figure 8. Frequency Response Showing Typical Variation Device to Device.

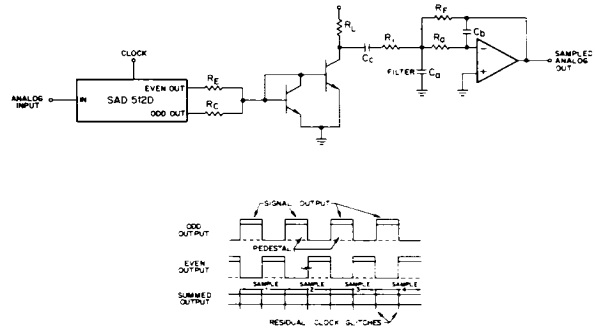

Figure 9. Normal Operating Configuration.

CIRCUIT CONFIGURATION

The normal operating configuration is shown in Fig. 9. The odd and even outputs are summed to provide continuous output and cancellation of the clock waveforms. The even output contains the same information as the odd output, only delayed for one-half clock period, or a total of 513 elements of delay. The data input, odd and even outputs, and summed output are also shown in Fig. 9.

A sync input is included on the device and the waveform is shown in Fig. 3. This input allows synchronized operation of multiple devices in either serial or parallel configuration when the same sync pulse is applied to each individual SAD-512D. If the devices are used individually the sync input (pin 7) should be grounded.

PERFORMANCE CONSIDERATIONS

The SAD-512D, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or correction, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency.

The analog input should be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable — to a limit more nearly 0.3 f_{sample}. The reason for this requirement is that all input components become modulated by the sampling frequency to generate ($f_s - f_{in}$) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear an equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components.

The output should be filtered because even after full-wave combination, the output is only stepwise continuous. Clocking steps and transient "glitches" appear at the times of clock transitions. The high frequencies contained in the abrupt changes and in the clocking glitches are all extraneous and for best performance should be removed by a filter with cutoff at approximately $f_{sample}/2$ or less and rolloff of as much as 36 dB/octave or more. Also, overload should be avoided because increased signal amplitude near overload gives rise to rapidly increasing high-order intermodulation products which lie within the useful pass band and which thus are not normally reducible by output filtering.

For optimized performance, care should be given to layout and design as well as to the filtering requirements. Ground planes are required on circuit boards to reduce cross-talk, and high-quality summing operational amplifiers are required to obtain maximum cancellation of clock pedestals and glitches.

For many applications, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved. For such relaxed requirements, a simple output circuit such as that shown in Fig. 10 is often useful.

DEVICE CHARACTERISTICS AND OPERATING PARAMETERS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Clock Voltage[1]	V_c	5		V_{DD}	Volts
Drain Supply Voltage[1]	V_{DD}	10	15	17	Volts
Control Bias Voltage[1]	V_{BB}		$V_{DD}-1$	V_{DD}	Volts
Sampling Frequency (½ External Clock Frequency)	f_s	0.0015	–	1.5	MHz
Clock Pulse Width	t_{cp}	200	$t_c/2$	t_c-200	ns
Signal Frequency Bandwidth (3db point)		See Fig. 8	300		KHz
Signal to Noise		See Fig. 5			
Distortion		See Fig. 6			
Gain[2]			.8		
Video Input Capacitance	C_{in}		15		pf
Video Input Shunt Resistance[3]	R_{in}	300			Kohms
Output Resistance	R_o	See Fig. 7			
Optimum Signal Input Bias[4]			4.2		Volts
Maximum Input Signal Amplitude		1	2		Volts p-p
Sync Pulse Amplitude		5		V_{DD}	Volts
Clock Input Capacitance	C_C		8		pf

Notes:

1. *All voltages measured with respect to GND (pin 2).*
2. *The value of gain depends on the output termination resistance. See Fig. 7.*
3. *Effective a-c shunt resistance measured at 1 MHz sample rate.*
4. *The input bias voltage varies slightly with the magnitude of the clock voltage (and V_{dd}) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 15-volt clocks.*

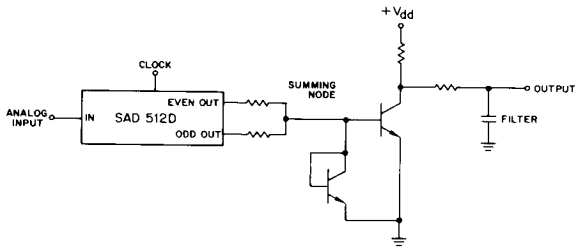

Figure 10. Simple Output Summing Amplifier.

EVALUATION CIRCUIT SC-512D

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the required filters, operational amplifiers, and ground plane. The schematic is shown in Fig. 11. The board provides a variable oscillator for sample frequencies from 20 KHz to 200 KHz. The output filter amplifier is designed as a two-pole, maximally flat filter with a cutoff frequency of 25 KHz. Change in cutoff frequency requires component changes. The balance control permits equalization of differences in source follower outputs.

The SC-512D board is designed to handle a wide range of bandwidths and clock rates; as a consequence anti-aliasing input filters should be externally provided to limit the input bandwidth to less than $f_{sample}/2$.

ABSOLUTE MAXIMUM VOLTAGES

TERMINAL	LIMITS	UNITS
Any terminal (with respect to GND)	+20 to –0.4	Volts

CAUTION

Static discharge to any lead of this device may cause permanent damage. Store with shorting clip or inserted in conductive foam. Use grounded soldering irons, tools, and personnel when handling devices. Avoid synthetic fabric smocks and gloves. It is recommended that the device be inserted into socket before applying power. Power supplies should not exhibit turn-on or turn-off spikes.

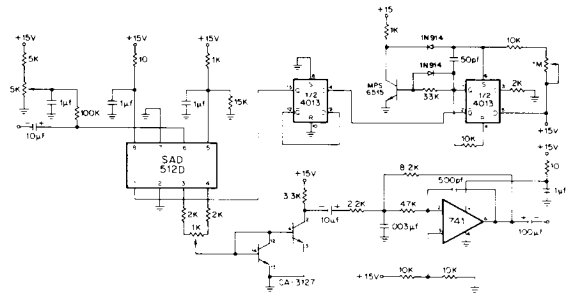

Figure 11. SC-512D Schematic Diagram.

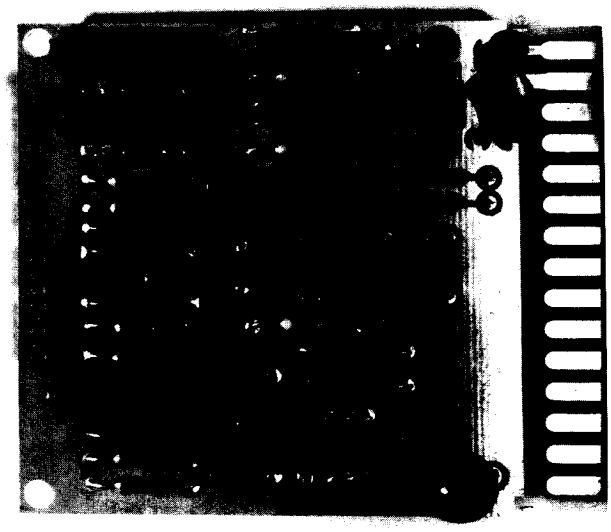

Figure 12. SC-512D Evaluation Circuit with SAD 512D Device.